WHAT IS CLAIMED IS:

1. A receiver apparatus comprising:

a demodulator for demodulating received radio signals into digital signals;

a mode selector for selecting either of a reproduction mode of reproducing the digital signals and an evaluation mode of evaluating the digital signals; and

an error generator for inverting a level of the digital signals for the evaluation mode at a predetermined timing to generate error data.

2. The apparatus in accordance with claim 1, wherein said mode selector comprises:

a first selector for selecting a destination of the digital signals; and

a second selector for selecting a source from either of said first selector and said error generator;

said first and second selectors synchronously selecting a same mode side.

3. The apparatus in accordance with claim 2, wherein said error generator comprises:

a pulse outputting circuit for outputting pulse signals at the predetermined timing; and

an inverter for inverting the level of the digital signals responsive to a transmission of the pulse signals.

4. The apparatus in accordance with claim 3, wherein said error generator comprises a preset value holding circuit which has a preset value defining a transmission timing of the pulse signals set from outside said apparatus to hold the preset value to supply the preset value to said pulse outputting circuit.

5. The apparatus in accordance with claim 1, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

6. The apparatus in accordance with claim 2, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

7. The apparatus in accordance with claim 3, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

8. The apparatus in accordance with claim 4, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

9. The apparatus in accordance with claim 1, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of

received data which follows the sync pattern and holds check data.

10. The apparatus in accordance with claim 2, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

11. The apparatus in accordance with claim 3, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

12. The apparatus in accordance with claim 4, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

13. The apparatus in accordance with claim 5, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

14. The apparatus in accordance with claim 9, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.

15. The apparatus in accordance with claim 10, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.

16. The apparatus in accordance with claim 11, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.

17. The apparatus in accordance with claim 12, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing

supplied from either of said error detector and said sync pattern detector.

18. The apparatus in accordance with claim 13, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.